Method and Structures for Increasing the Structure Density and the Storage Capacitance in a Semiconductor Wafer

The invention relates to a method for increasing a structure size of main structures - formed in essential parts in a depth of a semiconductor substrate - by means of an etching process which expands the main structures in the depth of the semiconductor substrate, provision being made of the semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching, and the main structures being arranged in checkered fashion in a rectangular surface grid, at a surface of the semiconductor substrate, in each case in alternation with secondary structures formed in each case essentially in a section of the semiconductor substrate that is near the surface.

RELATED ART

DRAM (dynamic random access memories modules are a mass-produced product with many applications. On the one hand, smaller dimensions and, on the other hand, a higher number of memory cells for storing data, that is to say an increasing storage density, are demanded of new generations of DRAM modules. This results in the need to further reduce the cell size of an individual memory cell, comprising a storage capacitance and a selection transistor. Depending on the arrangement of the storage capacitance in or above a metallization plane, a distinction is made between memory cells of the "stacked capacitor" type and "trench capacitor" type. In the case of a memory cell of

the "trench capacitor" type, a trench is formed in a monocrystalline semiconductor substrate of a semiconductor wafer below a metallization plane.

A dielectric, for example, a nitride/oxide layer system, is provided along the trench wall. In the monocrystalline semiconductor substrate, a region which is doped by outdiffusion, for instance, and adjoins the trench forms a first electrode. In the trench, a counterelectrode is formed by deposition of highly doped polycrystalline silicon.

Reducing the cell size leads to trenches with a smaller electrode area and thus to storage capacitances having a lower electrical capacitance. In order to compensate for the loss of capacitance, it is necessary to increase the capacitance again in a different way by means of complicated new process technologies. Examples thereof are a higher doping of the electrodes in order to reduce the charge carrier depletion, the use of dielectrics with a high dielectric constant and the application of additional structures (HSG, hemispherical grains) on the trench wall in order to enlarge the surface.

A further possibility for increasing the capacitance consists in increasing the surface of the trench by means of a bottle-like extension in a lower section of the trench. The trench thus extends in the depth of the semiconductor substrate also partly into regions of the semiconductor substrate located below the selection transistors formed on the surface of the semiconductor substrate.

Figure 4 shows plan view recordings taken by a scanning electron microscope, abbreviated to SEM hereinafter, of trenches of storage capacitances in different depths of a semiconductor substrate, said trenches being arranged in checkered fashion in alternation with unpatterned fields. The recordings each show an arrangement of structures which are based on a rectangular pattern in a mask layout and are transferred and etched into a semiconductor substrate in a conventional manner.

Figure 4a shows upper sections 8 of trenches of storage capacitances in the vicinity of the surface of the semiconductor substrate 6, said sections being provided with a protective layer that is resistant toward a bottle etching process.

A profile with a bottle-like extension 5 is shown in figure 4b is produced in each case in sections of the trenches formed below the protective layer. Between the sidewalls 7 of adjacent trenches, intermediate walls are formed from the material of the semiconductor substrate 6. The extent of the bottle-like extension 5 is limited by the demand for a minimum thickness of the intermediate walls. An excessively small thickness of the intermediate wall leads to a higher number of short circuits between the storage capacitances of adjacent memory cells on account of manufacturing tolerances.

Figure 4c represents the trenches in the region of a trench bottom 9 which terminates the trenches in the depth of the semiconductor substrate 6. They have a rectangular form with a smaller cross-sectional area than directly below the protective layer.

Overall, figure 4 reveals that although the electrode surface of the storage capacitance is enlarged by the bottle-like extension of the trench, on the other hand, the extent of the bottle-like extension is limited.

OBJECT OF THE INVENTION

Therefore, the invention is based on the object of providing a method and a structure with which it is possible to further increase a structure density and/or a storage capacitance of an individual structure in a semiconductor substrate compared with conventional methods and structures.

In the case of a method of the type mentioned in the introduction, the object is achieved according to the invention by means of the features mentioned in the characterizing part of patent clam 1. The object is furthermore achieved by means of a structure in accordance with paten t claim 14. Advantageous developments of the invention emerge in each case from the subclaims.

Thus, according to the invention, before an etching process which expands the main structure in the depth, the longitudinal and transverse extents of main structures in the depth of the semiconductor substrate are oriented in rotated fashion with respect to the x, y axes of the surface grid. As a result, the sections of the semiconductor substrate which are located below secondary structures are made available essentially completely for an extension of the main structures by means of the etching process which expands the main structure in the depth.

As a consequence, significantly larger dimensions and surfaces are possible for the main structures in the depth of the semiconductor substrate. If the main structures are formed in each case as electrical capacitances with electrode areas running along the surface, then it is possible to achieve higher capacitance values in comparison with conventional methods given the same space requirement on the surface of the semiconductor substrate by virtue of the better utilization of a volume of the semiconductor substrate. Given identical capacitance values, a large structure having the main and secondary structures can be embodied in a higher density by the method according to the invention.

The etching process which expands the main structure in the depth is referred to hereinafter, for simplification, as bottle etching process without this effecting are restriction to bottle etching processes in the narrower sense.

The term secondary structures also includes unpatterned sections of the surface of the semiconductor wafer.

One example of an alternate arrangement of main and secondary structures is a checkered arrangement (checkerboard). However, the method according to the invention does not necessarily presuppose the checkered arrangement of main and secondary structures. The longitudinal and transverse extents of the main structures are oriented in a manner rotated by essentially 45 degrees with respect to the x, y axes of the surface grid. A maximum utilizability of the sections of the semiconductor

substrate which are arranged below the secondary structures results in this case. Intermediate walls between adjacent main structures are then formed in cross-sectional planes parallel to the surface of the semiconductor substrate with approximately the same thickness.

The method according to the invention provides an area-selective etching process. To that end, provision is made of the semiconductor substrate comprising a crystalline material which has a crystal lattice with crystal faces that can be differentiated. In suitable etching processes, different etching resistances can be derived form the different properties of the crystal faces. The crystal lattice then has crystal faces that are less resistant to etching and crystal faces that are more resistant to etching.

Preferably, a large structure having at least the main structures is now imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces that are less resistant to etching.

Preferably, furthermore, the area-selective etching process is controlled in such a way that, in the depth of the semiconductor substrate below a structure edge determined by an extent of the secondary structures into the depth of the semiconductor substrate, primary sidewalls of the main structures that are constructed from the crystal faces that are less resistant to etching are substituted by secondary sidewalls constructed from the crystal faces that are more resistant to etching. The orientation of the crystal faces that are more resistant to

etching is rotated in customary semiconductor substrates with respect to the orientation of the crystal faces that are less resistant to etching, so that in this way the orientation - which is intended according to the invention and is rotated with respect to the surface grid - of the longitudinal and transverse extents of the main structure in the depth of the semiconductor substrate is achieved in a particularly advantageous manner.

The large structures are imaged onto the semiconductor substrate by means of a mask having an essentially rectangularly patterned mask layout.

The semiconductor substrate is preferably provided as a semiconductor wafer to be processed in semiconductor process technology. In the processing of the semiconductor wafer, a further advantage of the method according to the invention is exhibited in the fact that only one marking which identifies a crystal orientation in the semiconductor wafer and defines the position of the semiconductor wafer with respect to the mask has to be modified, to be precise in such a w ay that it is rotated by 45 degrees with respect to the conventional marking and, according to the invention, identifies the orientation of the crystal faces that are less resistant to etching. The processing of the semiconductor wafers, that is to say the process steps of lithography, dry etching and implantation, is then effected unchanged with respect to nonrotated semiconductor wafers corresponding to the prior art.

According to the invention, provision is to be made of the main structures at the surface of the semiconductor substrate in essentially oval fashion.

Monocrystalline silicon is preferably chosen as the material of the semiconductor substrate. For an area-selective etching process in the course of which <100> crystal faces are etched more rapidly than <110> crystal faces, the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

Preferably, in the course of a further processing of the semiconductor substrate, the main structures are functionally designed as storage capacitances and the secondary structures are essentially designed as selection transistors assigned to the storage capacitances.

The method according to the invention is explained in more detail below using the example of a storage capacitance for a DRAM memory cell:

A mask which prescribes the arrangement at least of main structures is provided with a rectangular pattern for patterning deep trenches each serving as a storage capacitance. The structures on the mask are imaged onto a semiconductor wafer provided with a marking according to the invention, which marking points in the <100> crystal orientation, by means of an exposure device. In this case, the longitudinal side of the imaged rectangles is oriented parallel to the <100> crystal orientation in the semiconductor wafer. The trenches are subsequently etched by means of a dry etching step whose etching speed is dependent on the crystal orientation, in the semiconductor wafer crystal faces with a <100> orientation being etched more rapidly than crystal faces with a <110> orientation. Only crystal faces with a <110> orientation then remain after a specific etching time. By means of a further

etching step, the deep trenches etched in the dry etching step are extended in bottle-like fashion below a trench depth of about one micrometer. Above one micrometer, the trenches are provided with an etching-resistant protective layer which prevents lateral etching into regions to the semiconductor substrate which are near the surface.

Before the bottle etching which leads to a bottle-like extension of the trench, the main structure which is produced in the course of the above-described method according to the invention in a semiconductor wafer is an etched trench which has, in an upper section adjoining the surface of the semiconductor wafer, a profile which is oval in plan view, with longitudinal sides parallel to the <100> crystal orientation, that is to say <100> sidewalls. IN a lower section below the protective layer, that is to say for instance below one micrometer, the trench has a square profile with <110> sidewalls. In this case, the length of the square diagonals essentially corresponds to the longitudinal extent of the oval profile in the upper part of the structure. The upper oval part of the structure is thus rotated by 45 degrees with respect to the lower square part since the two crystal orientations <100> and <110> are at an angle of 45 degrees with respect to one another.

In the case of the mask layout as used for the production of DRAM modules, the rectangles to be imaged are arranged in checkered fashion. The thickness of an intermediate wall between the sidewalls of the individual trenches is significantly increased compared with the semiconductor wafer processed in nonrotated fashion.

Hereinafter, checkered arrangement is understood to be a pattern in which the rectangles to be imaged on the mask are arranged in rows and are at the same constant distance from one another in each row. The rows are in each case arranged offset with respect to one another in such a way that, in the row lying below or above one row, two rectangles of said one row again have a rectangle situated between them essentially centrally. The distances between the rectangles are chosen such that the rectangles do not touch one another. By virtue of the square cross section and the rotated form of the lower part of the trenches, the volume in the semiconductor wafer is utilized significantly better compared with the conventionally processed semiconductor wafer.

After a further etching step having a duration of about 90 seconds, which brings about a bottle-like extension in the lower section of the trench, the trench in the depth of the semiconductor substrate has a profile that is square in plan view. The thickness of the intermediate walls comprising the semiconductor substrate between the individual trenches is of the order of magnitude of 100 nanometers, instead of about 20 nanometers in the case of semiconductor wafers processed in nonrotated fashion. It is thus possible to etch significantly larger extensions of the trenches, thereby increasing the electrical capacitance of storage capacitances formed from the trenches. Moreover, the square cross section of the lower part of the trenches leads to an optimum filling of the area of the semiconductor wafer in the depth of the semiconductor substrate.

In order to reduce leakage currents in a DRAM cell, comprising a selection transistor and a storage capacitance, the semiconductor wafer from which the DRAM cell is produced is processed according to the method according to the invention.

A similar method for reducing leakage currents is also described in WO 00/02249.

The required size of a storage capacitance depends, inter alia, on the leakage currents that occur. A typical value for a DRAM cell storage capacitance comprising a deep trench is the 40 fF/cell, in which the total cell leakage current is of the order of magnitude of 10 to 15 fA/cell. The latter contains various components, such as, for example, leakage currents through the dielectric, leakage currents along an interface between the semiconductor substrate and a structure that insulates the storage capacitance in the region near the surface (STI, shallow trench isolation), or leakage currents in the region of the interfaces of source and drain of the selection transistor.

In accordance with the method according to the invention for reducing leakage currents in a DRAM cell having a selection transistor and a storage capacitance, the leakage current along the interface between the semiconductor substrate and the STI structure is now significantly reduced. The reduction of the leakage current can be attributed to a lower density of defect locations (trap) along the interfaces oriented according to the invention, since the size of the leakage current is correlated with the number of defect locations and the

number of defect locations is reduced in the case of a changed crystal orientation.

A reduction of the total cell leakage current directly decreases the required capacitance. An advantage afforded by a lower capacitance is that the trench depth of the trench serving as capacitance can be reduced. As a result, the etching time could be reduced by the same order of magnitude as the trench depth, thereby significantly increasing the throughput of this process step.

Statistics based on examinations of a plurality of DRAM modules reveal that the total cell leakage currents of a DRAM cell in the case of the semiconductor wafer processed in a manner rotated by 45 degrees according to the invention are reduced by more than 30% compared with the semiconductor wafer processed in nonrotated fashion.

The reduction of the cell leakage current leads to an equivalent increase in the time interval after which the charge in one of the DRAM cells has decreased on account of leakage currents to an extent such that the charge stored in a memory cell has to be refreshed. This time interval is referred to as "retention time".

A DRAM cell containing a storage capacitance having a structure according to the invention in a semiconductor wafer which has been processed in accordance with the method according to the invention has an increased storage capacitance, reduced leakage currents and thus an increased "retention time".

EMBODIMENTS

The invention is explained below with reference to figures, identical reference symbols being used for mutually corresponding components. In the figures:

Fig. 1 shows a diagrammatic illustration of an arrangement comprising mask and semiconductor wafer for carrying out the method according to the invention,

Fig. 2 shows a diagrammatic illustration of an arrangement comprising mask and semiconductor wafer for carrying out a conventional method,

Fig. 3 shows a diagrammatic longitudinal section through a trench etched into semiconductor substrate,

Fig. 4 shows SEM plan view recordings of trenches in a semiconductor wafer in different depths,

Fig. 5 shows SEM plan view recordings of structures according to the invention in a semiconductor wafer in different depths,

Fig. 6 shows SEM plan view recording of structures according to the invention in a semiconductor wafer before and after a bottle etching in different depths,

Fig. 7 shows diagrammatic plan views of surfaces of a semiconductor substrate processed conventionally and of a semiconductor substrate processed according to the invention, and

Fig. 8 shows an illustration of the functional dependence of the number of discharge memory cells AS on the time TRet in the case of semiconductor wafers processed

according to the invention and in the case of semiconductor wafers processed conventionally.

For the method according to the invention, a mask 3 and a semiconductor wafer 1 made of monocrystalline silicon are arranged in the manner shown in figure 1. The semiconductor wafer 1 is provided with a marking 2 according to the invention, which marking is rotated by 45 degrees with respect to conventionally marked semiconductor wafers and identifies the <100> crystal orientation of the silicon. By means of the marking, the mask is oriented to the crystal orientation in the semiconductor wafer. The mask structure is thus imaged along a different crystal orientation compared with conventional methods.

For comparison purposes, an arrangement corresponding to the prior art is illustrated in figure 2. Here the semiconductor wafer 1 is provided with a marking 2 pointing in the <110> crystal orientation.

Figure 3 shows a structure which is etched into a semiconductor substrate 6 and is designed as a trench 4. On account of a further etching step below a trench depth of about one micrometer, the trench has a bottle-like extension 5 for enlarging an electrode area of a storage capacitance to be processed from the trench. The upper section of the trench 8 is provided with a protective layer which prevents lateral etching into the semiconductor substrate 6 in regions near the surface.

As already explained in the introduction, trenches of the type described can be seen in plan view in figure 4. The trenches were imaged onto a nonrotated semiconductor

wafer using a checkered mask layout and subsequently etched into the semiconductor substrate 6.

Figure 4a illustrates the upper parts - provided with a protective layer - of the trenches 8, the sidewalls of which form an oval and the long side of which is arranged parallel to the <110> crystal orientation. Such a side is called <110> sidewall 7 for short hereinafter.

Deeper in the semiconductor substrate, approximately where the protective layer ends, the cross section illustrated in figure 4b results, said cross section showing a bottle-like extension 5. Below the protective layer, the sidewalls form a rectangle with <110> sidewalls 7. Intermediate walls formed from the semiconductor substrate 6 between the sidewalls of the individual trenches 8 have, at their thinnest points, a very small thickness of approximately 20 nanometers, which can lead to short circuits in the case of trenches processed to form storage capacitances, on account of manufacturing tolerances.

Figure 4c represents the trenches in the region of a trench bottom 9 terminating the trenches in the depth of the semiconductor substrate. There they have a rectangular form with a smaller cross-sectional area than directly below the protective layer. The sidewalls are again <110> sidewalls 7.

The trenches shown in figure 5 were produced by the method according to the invention. They are based on the same checkered mask layout of figure 4. For this purpose, the mask layout is imaged onto a semiconductor wafer

oriented according to the invention. Afterward, the trenches are etched into the semiconductor substrate 6 and each provided with a protective layer in upper sections. Figures 5a to 5d illustrate cross sections of the trenches in different depths parallel to the surface 10 of the semiconductor substrate 6.

In this case, figure 5a shows a plan view of the trenches at the surface 10 of the semiconductor substrate 6. Figure 5b shows a cross section through the trenches in the region of the protective layer below the surface 10. The sidewalls of the upper sections of the trenches in each case form an oval whose long sides are oriented according to the invention parallel to the <100> crystal orientation. Such a side is called <100> sidewall 11 for short hereinafter. Figures 5c and 5d represent the cross sections of the trenches below the protective layer 12 in two different depths. The sidewalls of the trenches form a square with <110> sidewalls 7 in cross section. The sidewalls of the upper section of a trench are thus rotated by 45 degrees with respect to the sidewalls of the lower section of the same trench. As can be seen when comparing figure 4c with figure 5d, the resulting rotated square cross section of the trenches in the region below the protective layer leads to an improved utilization of the area of the semiconductor substrate 6.

The improved utilization of area becomes clear from figure 6. The cross sections of the trenches produced according to the invention in figures 6a to 6c were recorded before the etching step (bottle etch) - leading to the bottle-like extension - in different depths and

correspond to the cross sections of the trenches in figures 5b to 5c.

The cross sections of the trenches after the etching step leading to the bottle-like extension can be seen on a larger scale in figures 6d to 6f. The cross section - oval in plan view - in the upper section of the trenches with <100> sidewalls 11 is shown in figure 6d. Figures 6e and 6f show the square cross sections with <110> sidewalls 7 of the bottle-like extensions in two different depths, one above and one below the trench center. The perfect utilization of area in the depth of the semiconductor substrate can clearly be discerned here.

The better utilization of a semiconductor substrate 6 by the method according to the invention is also illustrated with reference to figure 7.

A pattern of main and secondary structures 131, 132 is formed on a surface of the semiconductor substrate 6, said pattern being oriented along a surface grid 14. The main and secondary structures 131, 132 are arranged alternately in checkered fashion in the surface grid 14.

The surface grid 14 forms equally sized square fields 151, 152 in this example for illustration purposes. However, the method according to the invention also leads to an advantageous utilization of the semiconductor substrate 6 in the case of other divisions with unequally sized or expanded fields.

The secondary structures 132 are essentially arranged in a section of the semiconductor substrate 6 near the surface between the surface of the semiconductor substrate

6 and a structure edge in the depth of the semiconductor substrate 6. By contrast, substantial parts of the main structures 131 are formed below the structure edge. The main structures 131 are conventionally expanded below the structure edge by means of a bottle etching process. After being expanded, the main structures 131 also extend, as illustrated in figure 7a, into sections of the semiconductor substrate 6 which lie below the secondary structures 132.

In this case, the bottle etching process extends the main structures 131 in a manner independent of direction, so that the maximum possible extension of a main structure 131 is also restricted in the depth of the semiconductor substrate 6 to a field 151 assigned to the main structure 131. Sections of the semiconductor substrate which extend below the structure edge under fields 152 assigned to the secondary structures remain unused.

By contrast, those sections of the semiconductor substrate 6 below the substrate edge which are arranged below the fields 152 assigned to the secondary structures 132 are also made available, by the method according to the invention, for extension of the main structures 131.

For this purpose, as illustrated in figure 7b, the surface grid 14 is oriented parallel to crystal feces of the semiconductor substrate 6 that are less resistant to etching. In the course of an area-selective etching process, the main structures 131 are formed in the depth of the semiconductor substrate 6 below the structure edge with sidewalls that are ideally rotated by 45 degrees with respect to the surface grid 14. If the rotated main

structures 131 are subsequently expanded by means of a bottle etching below the structure edge, then an extended field 161 results for each main structure 131 as maximum extension.

The semiconductor substrate 6 below the structure edge can be completely assigned to the extended fields 161 and can thus advantageously be utilized almost completely for the extension of the main structures 131.

Figure 8 illustrates the functional dependence of the number of discharged memory cells AS on the time tRet - referred to as "retention time" - for DRAM modules produced from semiconductor wafers processed in rotated fashion according to the invention and from semiconductor wafers processed in non rotated fashion. Two DRAM modules in each case were examined for each curve. Curves A and B show the behavior of DRAM modules from semiconductor wafers processed in nonrotated fashion, curve B concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve A. Curves C and D show the behavior in the case of semiconductor wafers processed in rotated fashion according to the invention, curve D again concerning memory cells having a storage capacitance reduced by 10% compared with the memory cells of curve C. The significantly shallower profile of curves C and D compared with curves A and B describes a lengthened "retention time" in the case of semiconductor wafers processed in rotated fashion. The influence of the magnitude of the storage capacitance on the "retention time" also becomes clear from curves Band D. A reduced storage capacitance is accompanied by a decrease in the

"retention time". In a time interval of 128 ms < tRet < 8 sec, the following holds true: AS in the case of semiconductor wafers processed in rotated fashion is approximately 0.5* AS in the case of semiconductor wafers processed in nonrotated fashion.

List of reference symbols

1	Semiconductor wafer
2	Marking
3	Mask
4	Trench
5	Extension
6	Semiconductor substrate
7	<110> sidewall
8	Upper part of the trench
9	Trench in the region of the trench bottom
10	Trench at the surface
11	<100> sidewall
12	Trench below the protective layer
131	Main structure
132	Secondary structure
14	Surface grid
151	Field for main structure

152 Field for secondary structure

161 Field for main structure below structure edge

PATENT CLAIMS:

1. Method to increase the structure size of main structures (131) being substantially formed into a depth of a semiconductor substrate (6) by an etch process widening the main structures (131) in the depth of the semiconductor substrate, wherein the main structures (131) are arranged at a surface of the semiconductor substrate (6) alternating with a secondary structure being substantially formed in a portion of the semiconductor substrate (6) close to the surface in a surface grid (14) and aligned in a longitudinal and transversal direction parallel to x, y axes of the surface grid (14),

characterized in that

- the lateral and transversal directions of the main structures (131) in the depth of the semiconductor substrate (6) are rotated relative to the x, y axes c, and thereby

- the portions of the semiconductor substrate (6) below the secondary structures (132) are substantially completely made available for the formation of the main structures (131) by means of the widening etch process.

2. Method of claim 1, characterized in that the lateral and transversal directions of the main structures (131) are rotated relative to the x, y axes of the surface grid (14) by 45 degrees.

3. Method of claim 1 or 2, characterized in that the semiconductor substrate (6) comprises a crystalline material with a lattice and crystal face having differing etch resistance and the rotation of the lateral and transversal directions of the main structures (131)

relative to the surface grid (14) comprises an etch process being selective with regard to the crystal face.

4. Method of claims 1 to 3, characterized in that at least one overall structure defining the main structures (131) is projected by an exposure apparatus onto the surface of a semiconductor surface (6) with the x, y axes of the surface grid (14) being parallel to less etch resistant crystal faces of the semiconductor substrate (6).

5. Method of claim 4, characterized in that a mask (3) comprising a rectangular structured mask layout of the overall structure is aligned to the less etch resistant crystal faces of the semiconductor substrate (6) prior to the projection.

6. Method of claims 3 to 5, characterized in that the semiconductor substrate (6) comprises a semiconductor wafer (1) and a marking (2) indicating a crystal orientation of the crystal lattice is provided to the semiconductor wafer (1).

7. Method of claim 6, characterized in that the marking (2) indicates a crystal orientation of a less etch resistant crystal face.

8. Method of claim 7, characterized in that the marking (2) is used to aligned the mask (3) in the exposure apparatus in a conventional fashion.

9. Method of claims 1 to 8, characterized in that the main structures (131) are provided at the surface of the semiconductor substrate (6) with an oval cross-section.

10. Method of claims 1 to 9, characterized in that the material of the semiconductor substrate (6) comprises monocrystalline silicon.

11. Method of claim 10, characterized in that the surface grid (14) is aligned to the <100> orientation of the monocrystalline silicon.

12. Method of claim 11, characterized in that the <100> crystal faces with less etch resistance are etched faster than the <110> crystal faces with higher etch resistance during the face selective etch process.

13. Method of claims 1 to 12, characterized in that the main structures (131) are provided with a protective layer being at least resistant against the widening etch, the protective layer been formed in upper portions of the main structures (131) between the surface of the semiconductor substrate (6) and at least a lower edge of the secondary structures.

14. Method of claims 1 to 13, characterized in that the main structures (131) are functionally formed as storage capacitors.

15. Method of claims 1 to 14, characterized in that the secondary structures (132) are functionally formed as access transistors adjoining the storage capacitors.

16. Structure formed in a semiconductor substrate (6) according to a method of the claims 12 to 15, characterized in that the structure comprises a trench (4) with an oval profile in a cross-section in an upper portion adjoining the surface of the semiconductor substrate (6), the profile

comprising a longitudinal direction parallel to the <100> crystal orientation, the trench comprising a substantially rectangular profile in a lower portion arranged below an etch resistant protection layer with side walls parallel to the <110> crystal orientation.

17. Structure of claim 16, characterized in that the protection layer extends to a maximum of one micro meter below the surface of the semiconductor substrate (6).

18. Structure of claim 16 or 17, characterized in that the trench comprises a bottle shaped extension (5) in the lower portion with a quadratic profile in plan view having side walls parallel to the <110> crystal orientation.

19. Arrangement of structures according to one of the claims 16 to 18, characterized in that the thickness of remaining walls between neighboring structures (131) in the semiconductor substrate (6) is in the order of 100 nm.

20. Arrangement of claim 19, characterized in that the structures are formed as storage capacitors.

21. Method to reduce the leakage current in a DRAM cell comprising an access transistor a storage capacitor, characterized in that a semiconductor wafer (1) comprising the DRAM cell is processed according to a method of one of the claims 6 to 15.

22. DRAM cell manufactured with the method of claim 21, characterized in that the storage capacitor comprises a structure of one of the claims 16 to 18.

ABSTRACT

Method for increasing the structure density and/or the storage capacitance of structures to be introduced into a semiconductor wafer (1), the semiconductor wafer having a marking (2) prescribing a breaking direction and the structures being imaged onto the semiconductor wafer (1) by means of an exposure device and a mask (3), whose mask layout prescribes the structures. The semiconductor wafer (1) is rotated by 45 degrees in its plane with regard to the mask layout prior to the imaging of the structures and provided with a marking (2) prescribing a new breaking direction parallel to a <100> crystal orientation. The further process steps take place unchanged with respect to nonrotated semiconductor wafers.